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Buffer scheme with battery energy storage capability for enhancement of network transient stability and load ride-through

X.Y. Wang, D.M. Vilathgamuwa*, S.S. Choi

School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798, Singapore

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Abstract

This paper examines a buffer scheme to mitigate the negative impacts of power-conditioned loads on network voltage and transient stabilities. The scheme is based on the use of battery energy-storage systems in the buffers. The storage systems ensure that protected loads downstream of the buffers can ride through upstream voltage sags and swells. Also, by controlling the buffers to operate in either constant impedance or constant power modes, power is absorbed or injected by the storage systems. The scheme thereby regulates the rotor-angle deviations of generators and enhances network transient stability. A computational method is described in which the capacity of the storage systems is determined to achieve simultaneously the above dual objectives of load ride-through and stability enhancement. The efficacy of the resulting scheme is demonstrated through numerical examples.
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Keywords: Battery energy-storage system (BESS); Power buffer; Power quality; Transient stability; Load ride-through

1. Introduction

The stability of power systems has always been an important consideration, especially when it involves the transmission of power over long distances. The problem has been compounded somewhat in recent years as a significant proportion of present-day industrial loads are equipped with power-conditioning capabilities. These loads usually draw constant power regardless of their terminal voltage level. In the event of a fault in the power system, the depressed voltage will result in an increase in the load current. This would lead to an increase in the voltage drop across the source impedance, which in turn causes a further decrease in load terminal voltage. Load voltage stability would be impacted negatively if no countermeasures were taken. Furthermore, constant-power loads also affect rotor-angle stability of power systems, in a manner that can be very much different if the loads were to behave like a constant-impedance type. Hence, it is not surprising that load modelling and the impacts of loads on power systems are attracting the interest of many researchers [1–3].

In an attempt to address the above-mentioned stability problem due to the presence of constant-power loads, the authors have proposed [4] the use of a power buffer system through which the loads are supplied. The buffer consists of two back-to-back converters interconnected by a DC-link. During a fault, the input impedance (viewed from the source side) of the buffer–load combination is controlled by the front converter to maintain an impedance value identical to that under the pre-fault condition. In this way, the threat of an increase in the load current during the fault event is alleviated. An energy-storage system was connected across the DC-link [4] and its role was to supply the shortfall in real power between that supplied from the upstream system and the (constant) load demand. The buffer design was extended [5] to cater for unbalanced faults, with the buffer controller designed to mitigate negative phase sequence voltage under the fault condition. The scheme allows not only the load to ride through the fault event but also alleviates the threat of voltage instability.

* Corresponding author. Tel.: +65 67906461; fax: +65 67912687.
E-mail addresses: wang0089@ntu.edu.sg (X.Y. Wang), emahinda@ntu.edu.sg (D.M. Vilathgamuwa), esschoi@ntu.edu.sg (S.S. Choi).

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The success of such a buffer system must include a suitable energy-storage system to compensate for any of the mismatch in power between the constant-load demand and that supplied by the upstream system, during and following the fault disturbance. This aspect of buffer design was not analyzed in reference [4]. Indeed, the energy-storage capacity aspect of the buffer scheme is one main design factures to be addressed in the study presented here. The design will be expanded to a proposed network stabilization scheme. It will be shown that the scheme is capable of extending the function of the buffers described in references [4,5]; it can help in achieving the dual purpose of network transient stability enhancement while maintaining supply quality to the load. The examined power system is described in Section 2. The operational principle of the buffer scheme and a method to determine the capacity of the storage system necessary to ensure the success of the scheme are also given. Numerical examples are used in Section 3 to illustrate the application of the proposed scheme.

2. Model development

Although practical power systems are highly complex, the generic two-generator power system network shown in Fig. 1 is convenient to use for illustrating the operating principle of the buffer scheme. Indeed, there are radial networks that can be approximated by the network model, as shown in reference [6]. One can consider the practical situation in which a group of generators, represented by the equivalent unit G_2, is interconnected with another group of generators, represented by an equivalent unit G_1, through the transmission link between Buses 1 and 2. The power outputs of G_1 and G_2 are denoted as P_{G_1} and P_{G_2}, respectively. Losses in the transmission system are assumed to be negligible. As the focus of this work is on the buffer scheme, details of the generators and their control systems will not be described here; although, in Section 3 the illustrative examples do include detailed model representations.

In the present problem formulation where power electronics-based devices have been increasingly used in the power systems, one recognizes some load demands would be considered essential. The nature of these demands would be such that supply to them must not be disrupted under specified momentary voltage disturbance conditions. Indeed, consideration for supplying such loads has given rise to the idea of Custom Power and the concept of a Power Quality Control Centre [7,8]. In whatever form, provisions would have to be made in the networks so that these loads, denoted as S_1 and S_2 in Fig. 1, can ride-through such voltage sag–swell disturbances. Hence, S_1 and S_2 would draw constant real powers P_{S_1} and P_{S_2}, respectively, regardless of the status of the power system. To ensure S_1 and S_2 real power demands are met, the provision considered in this work is through the arrangement of the buffers, as shown in the figure. More will be said about the buffer scheme later. The remaining loads D_1 and D_2 at the respective Buses 1 and 2 have no such stringent power requirement. The steady-state powers drawn by these loads are denoted as P_{D_1} and P_{D_2}. D_1 and D_2 could be assumed to be of constant-impedance type in this network model.

Having met the demands P_{S_1} and P_{D_1}, it is assumed Bus 1 has surplus generation from G_1, while Bus 2 has insufficient infeed from G_2 to meet the demands P_{S_2} and P_{D_2}. The deficiency is imported from G_1, via the link, by the amount P_{12}. Therefore, the steady-state power flow pattern is as shown in Fig. 1.

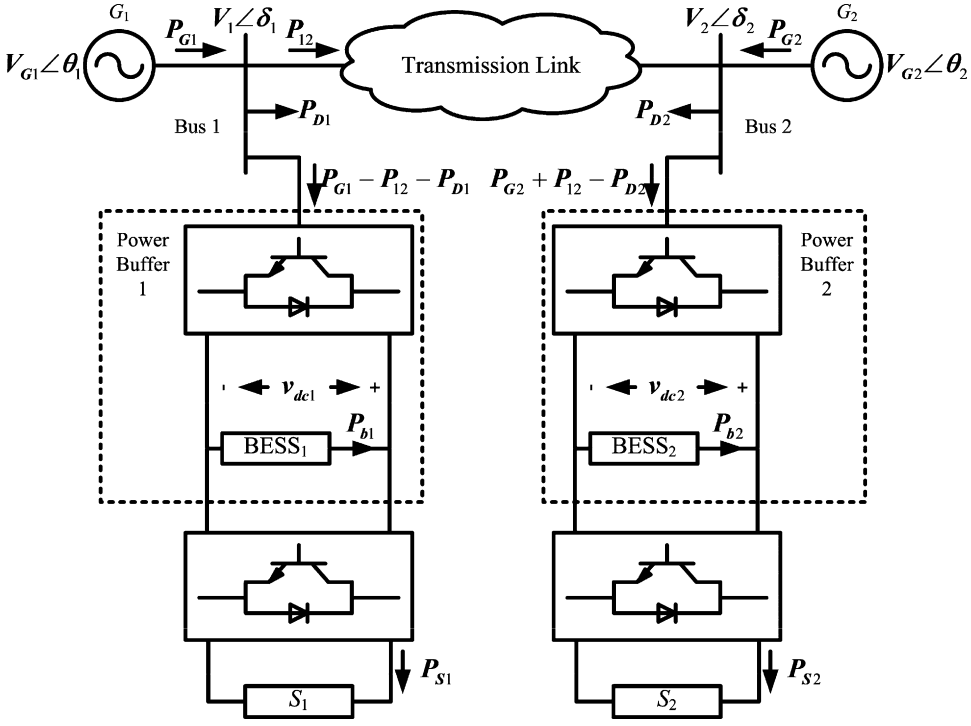

Fig. 1. Schematic diagram of two-generator network system with power buffers.

2.1. Buffer scheme to achieve improved load ride-through

Next, consider the function of the buffers. In the proposed scheme, the power buffers can be based on electronically controlled power converters. Under healthy system conditions, the buffers operate under the constant-power mode to meet the demands P_{S_1} and P_{S_2}, through control of the respective front-end converter while maintaining the DC-link voltages, v_{DC_1} and v_{DC_2}, at their nominal levels. This will ensure proper operation of the downstream converter-loads S_1 and S_2. It is through the control actions of the converters that S_1 and S_2 will enjoy excellent supply quality—an attribute similar to that described in reference [8] for so-called super-premium loads.

When a fault occurs in the transmission link, the voltage in the network will be depressed. To avoid the negative influence of constant power loads on system voltage stability, the power buffers may be switched into constant impedance mode by adjusting the PWM control signal [5]. Under such a condition, however, the power supplied from the utility to the downstream constant power loads will be reduced. Therefore, the impacts of the constant demands P_{S_1} and P_{S_2} on the buffers should also be considered.

As stated above, over these instances when the buffer(s) have to operate under constant-impedance mode while demands P_{S_1} (or P_{S_2}) have to be satisfied, the shortfall between P_{S_1} (or P_{S_2}) and the power supplied by the upstream utility has to be met. This is achieved by drawing power from the energy-storage systems within the buffer systems. Several possible storage media such as supercapacitors and flywheels could be used. In this investigation a, lead–acid battery energy-storage system (BESS) has been considered. This is because the lead–acid battery is one of the most cost-effective and well-established technologies for large-scale energy-storage [9]. The BESSs are shown connected across the DC-link of the buffers in Fig. 1.

2.2. Buffer scheme to achieve stability enhancement

With the above-described power buffers installed, their function can be extended to act as load dampers or stabilizers [5]. The operation scheme of the power buffer in enhancing system transient stability is addressed as follows.

From the instant of the fault inception and the initial transient period of (say) a few seconds, the governor control systems of G_1 and G_2 will generally be too slow to respond appreciably. Thus, the input mechanical powers to the generators can be considered constant. On the other hand, the excitation systems would usually be able to adjust the respective generator internal emf, since the control systems are designed to regulate the terminal voltage of the generators. Even with the actions of the excitation systems, however, a severe fault would cause the power P_{12} transmitted through the link to be greatly reduced. If both S_1 and D_1 were to behave like a constant-impedance type, Bus 1 load demand would also reduce as the load terminal voltage is depressed during a fault. Therefore, the surplus energy resulting from the constant input mechanical power and the reduced output electrical power P_{G_1} will accelerate the rotor of G_1. To reduce the power imbalance at Bus 1 and since S_1 is of a constant-power type, it is proposed that when the G_1 rotor accelerates during a fault, Power Buffer 1 will be designed to operate under a constant-power mode. In this way, the load demand at Bus 1 will be higher than that without the buffer. This will reduce the acceleration of G_1.

To change the buffer operation mode based on G_1 rotor speed may pose some implementation difficulty since G_1 is an equivalent of a cluster of generators. The precise meaning of rotor speed will need further careful consideration. As an alternative to rotor speed, the transfer power P_{12} can be used instead to identify the case of acceleration or deceleration of G_1. When a fault occurs and P_{12} reduces, G_1 accelerates and the operation mode of Buffer 1 is switched into constant-power mode to reduce the acceleration. Conversely, when P_{12} increases above its pre-fault level, Buffer 1 is then switched into constant-impedance mode.

At Bus 2, the situation is the reverse of that of Bus 1: when P_{12} reduces and without Buffer 2, G_2 would decelerate with respect to G_1. This is the classical 2-machine transient stability situation. Depending on the pre-fault power transfer level and fault clearing time (among other factors), there is a danger G_1 and G_2 may go into a first-swing instability condition. Hence, to mitigate the possibility of instability, Buffer 2 will be designed to operate under a constant-impedance mode during a fault so that Bus 2 total load demand will be reduced. In this way, the deceleration in G_2 would be less compared with the case without Buffer 2, because in the latter case, the constant-power demand P_{S_2} has to be met by an increase in P_{G_2} since P_{12} is reduced. Thus, by forcing Buffer 1 into a constant-power mode and Buffer 2 into constant-impedance mode during a fault, the rotor speed difference, and therefore the rotor-angle difference, between G_1 and G_2 can be reduced compared with to the case when the buffers are not used.

The buffers can also be designed to operate on the same principle following fault clearance when the network readjusts its bus voltages and power flows. When P_{12} reduces and there is accelerating power acting on G_1 to increase the generator speed, Power Buffer 1 is to operate under a constant-power mode. Conversely, when P_{12} increases and the generator decelerates, the buffer is switched to a constant-impedance mode. The role of Buffer 2 is to regulate the speed of G_2 in a similar manner. Repeated switching between the two buffer modes continue until the network settles into a new steady-state operating condition. Hence, it would appear that P_{12} variations can be used to control effectively the operating modes of the buffers.

2.3. DC-link voltage constraint

In the scheme, the buffers function to guarantee a constant power supply to S_1 and S_2. For example, when Buffer 1 operates under a constant-impedance mode, $BESS_1$ supplies any shortfall in power for S_1 when the network voltage is depressed. This will decrease the buffer DC-link voltage v_{DC_1}. To ensure S_1 voltage quality is not affected, however, v_{DC_1} has to be kept within certain limits, denoted by the range $[v_{DC,lower}, v_{DC,upper}]$,

or the inverter associated with S_1 will operate outside its control range. If the latter case occurs, the inverter protection system will be triggered and the supply to S_1 will be disrupted. This situation must be avoided. The extent v_{DC_1} will deviate from its nominal value depends very much on the capacity of $BESS_1$. Similar statements can be made concerning $BESS_2$. Hence, it is necessary to determine the respective BESS capacity in order that the buffers help S_1 and S_2 loads ride through the worst fault conditions of the scheme. In this way, the power buffers will ensure both stability enhancements while the supply quality to the loads will be guaranteed. Next, a method to determine the BESS capacity will be described.

2.4. BESS model description

Several models that can be used to describe the behaviour of a battery cell have been proposed by researchers [10–12]. The model proposed in reference [10] pertaining to a lead–acid battery cell has been selected for incorporation in the present buffer scheme. The reason for the selection is because the focus is on transient stability enhancement; the timescale of interest is well within the so-called short-term response characteristics of the battery cell model given in reference [10]. The adopted cell circuit model is reproduced in Fig. 2(a). As shown, $E_{b,i,j}$ is the cell open-circuit voltage, internal resistance $R_{S,i,j}$ represents the ohmic resistance due to polarization in the cell, and $R_{p,i,j}$ and $C_{p,i,j}$ are used to describe the discharge transfer loss and dynamics between parallel plates of electrodes and electrolyte, respectively.

In Fig. 2(b), the typical response of the cell terminal voltage $v_{b,i,j}$ to a step cell current change $i_{b,i,j}$ is shown. It is noted that a step increase in $i_{b,i,j}$ would result in the cell terminal voltage $v_{b,i,j}$ decreasing almost instantaneously before it approaches its steady-state value in an exponential manner. In describing this behaviour, the change in battery cell terminal voltage due to the step current has been described in reference [10] in the following way:

$$v_{b,i,j} = E_{b,i,j} - R_{s,i,j} i_{b,i,j} - R_{p,i,j} i_{b,i,j} (1 - e^{-t/\tau_{i,j}}) \quad (1)$$

where $\tau_{i,j}$ is the time constant of battery cell and

$$\tau_{i,j} = R_{p,i,j} C_{p,i,j} \quad (2)$$

Typically, $\tau_{i,j}$ is of the order of 0.2 s to a few seconds, depending on the magnitude of the step current change. Table 1 shows

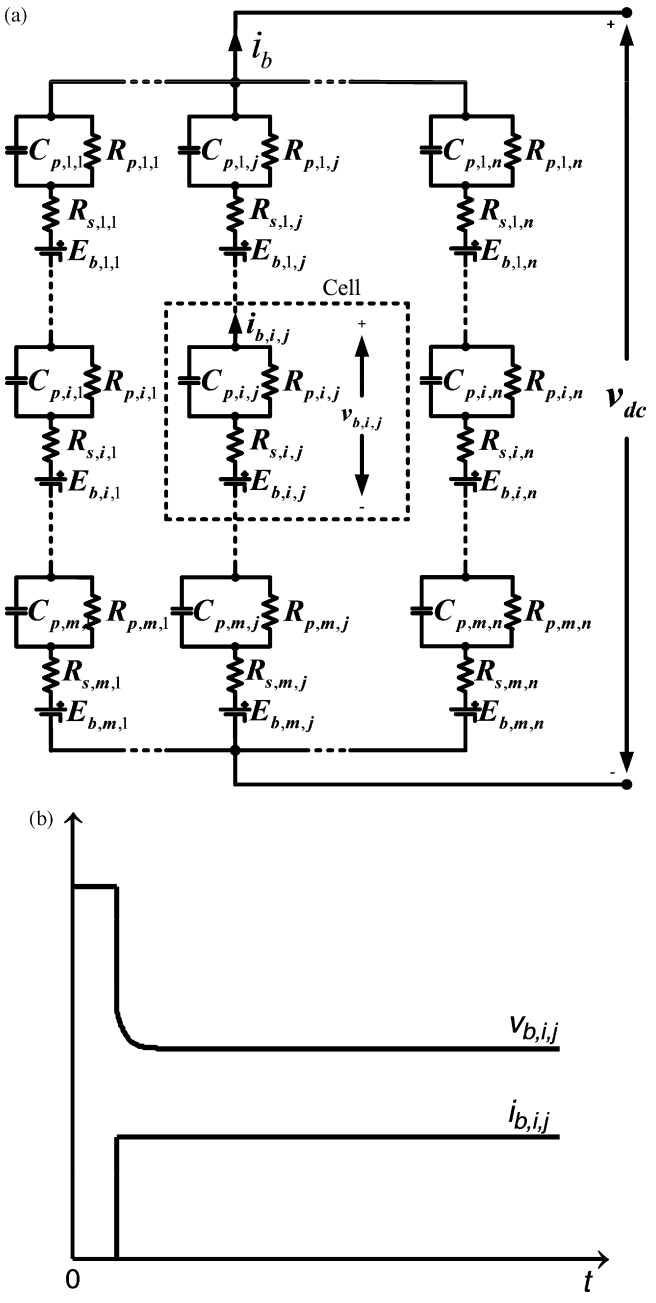

Fig. 2. (a) Schematic showing interconnection of lead–acid battery cells in BESS and (b) typical response of battery cell terminal voltage $v_{b,i,j}$ to step change in cell current $i_{b,i,j}$.

Table 1
Battery parameters used in simulations

ΔI (A)	R_S (Ω)	R_p (Ω)	C_p (F)	τ (s)
25	0.005	0.015	20	0.3
50	0.008	0.003	900	2.7
100	0.0052	0.003	1000	3
200	0.0032	0.002	1000	2
400	0.0022	0.001	750	0.75
600	0.002	0.0008	600	0.48
800	0.0018	0.00075	400	0.3
1000	0.0015	0.0007	200	0.14

the typical parametric values of the cell resistances and capacitance [10] and the corresponding $\tau_{i,j}$.

Assume the BESS has m cells connected in series in each string and a total of n parallel strings, as shown in Fig. 2(a). Assume the mn cells are identical; the characteristic of the ith series cell on the jth parallel string of the BESS is described by Eqs. (1) and (2). The BESS terminal voltage is denoted by v_{DC} since the BESS is connected directly across the DC-link of the buffer system. The BESS equivalent circuit, based on Fig. 2(a), is given in Fig. 3, where the BESS internal parameters E_b, R_S, R_p and C_p can be expressed in terms of the cell parameters as

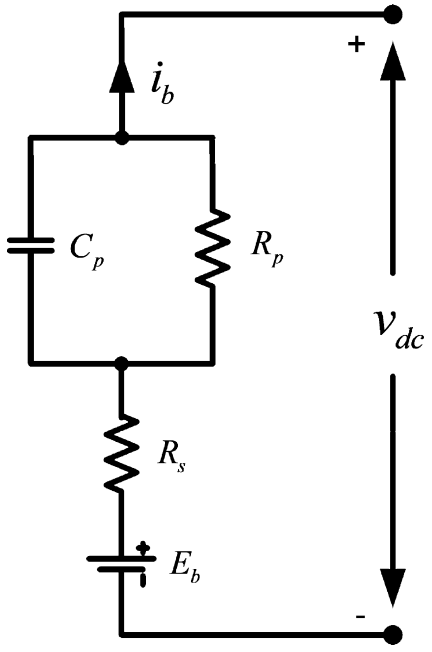

Fig. 3. Equivalent circuit of BESS.

follows:

$$\left.\begin{aligned} E_b &= mE_{b,i,j}/n \\ R_s &= mR_{s,i,j}/n \\ R_p &= mR_{p,i,j}/n \\ C_p &= nC_{p,i,j}/m \end{aligned}\right\} \tag{3}$$

In the manner similar to Eq. (1), the BESS terminal voltage $v_{DC}(t)$ can be described in terms of the BESS parameters and following a step change of the BESS current i_b as

$$v_{DC} = E_b - R_s i_b - R_p i_b(1 - e^{-t/\tau}) \tag{4}$$

where τ is the time constant of the BESS and

$$\tau = R_p C_p \tag{5}$$

The circuit model of the BESS is amendable for analysis, except for one complication. In adopting the equivalent circuit model, it has been stated earlier that the cell resistance and capacitance values are not constant but are functions of the magnitude of the current step. In fact, the state-of-discharge of the cell and temperature at which the cells operate at also affect the parametric values. Fortunately, the latter two factors could be considered constant over a fault disturbance event because the duration of the fault and its clearance is usually too short for the battery temperature and discharge state to vary appreciably. In this way, the values of the parameters would only depend on the magnitude of the discharge current step. In what follows, it will be assumed that the parametric values of R_S, R_p and C_p would be known for given magnitude of the current step. The information can be obtained either from the cell manufacturer or through experimental measurements.

2.5. DC-link voltage determination

As explained in Section 2.3, it is important that the DC-link voltages must be maintained within limits. Using the equivalent circuit model developed earlier, the BESS terminal voltage can be determined as follows. In the study of transient stability and in a step-by-step manner, the quantities $P_{12}(t)$, $P_{G_1}(t)$ and $P_{G_2}(t)$ are readily calculated. At Buses 1 and 2, P_{S_1} and P_{S_2} are known constants, whereas P_{D_1} and P_{D_2} vary with the square of the magnitude of the respective bus voltage. The BESS output powers $P_{b_1}(t)$ and $P_{b_2}(t)$ can therefore be calculated as follows:

$$\left.\begin{aligned} P_{b_1}(t) &= P_{S_1} - P_{G_1} + P_{12} + P_{D_1} \\ P_{b_2}(t) &= P_{S_2} - P_{G_2} - P_{12} + P_{D_2} \end{aligned}\right\} \tag{6}$$

Consider one of the buffers and omit the subscript 1 or 2 to simplify the expressions that follow. Approximate the continuous function $P_b(t)$ over the interval of interest T by a series of $N+1$ values: $P_{b(0)}$, $P_{b(1)}$, …, $P_{b(k)}$, …, $P_{b(N)}$ at times $t_{(0)}$, $t_{(1)}$, … $t_{(k)}$, …, $t_{(N)}$. Fig. 4 shows the $(k-1)$th, kth and $(k+1)$th intervals. Assume a uniform time interval so that each segment is of duration:

$$\Delta t = \frac{T}{N}$$

In this way, $P_b(t)$ may then be approximated by N pulses, each of duration Δt, and the magnitude of each pulse is given by:

$$\bar{P}_{b(k)} = \frac{(P_{b(k-1)} + P_{b(k)})}{2} \qquad k = 1, 2, \ldots, N \tag{7}$$

Hence, $\bar{P}_{b(k)}$ will be the power pulse applied over the kth time interval. Accordingly, the battery current step change due to $\bar{P}_{b(k)}$ is:

$$\bar{I}_{b(k)} = \frac{\bar{P}_{b(k)}}{v_{DC(k-1)}} \qquad k = 1, 2, \ldots, N \tag{8}$$

where $v_{DC(k-1)}$ is the BESS terminal voltage at the end of the $(k-1)$th time interval.

Next, $v_{DC(k)}$ can be generated through the following step-by-step and iterative method. Consider v_{DC} at the end of the first

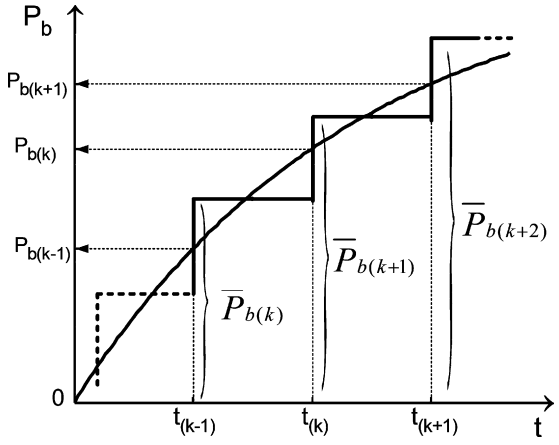

Fig. 4. Approximate $P_b(t)$ by individual power pulses $\bar{P}_{b(k)}$.

time step, i.e., $k=1$. The initial BESS terminal voltage is given by $v_{DC(0)} = E_b$, assuming the battery current is zero initially and the BESS open-circuit voltage is known. As shown in Fig. 5, assume the first power pulse, $\bar{P}_{b(1)}$, is positive. From Eq. (8), the corresponding battery current step change is given by:

$$\bar{I}_{b(1)} = \frac{\bar{P}_{b(1)}}{v_{DC(0)}} \tag{9}$$

With the known step current, one can utilize the corresponding BESS parametric values, denoted as $R_{S(1)}$, $R_{p(1)}$ and $C_{p(1)}$, to determine the DC-link voltage at the end of the first time interval using Eq. (4), i.e.,

$$v_{DC(1)} = v_{DC(0)} - R_{S(1)}\bar{I}_{b(1)} - R_{p(1)}\bar{I}_{b(1)}(1 - e^{-(\Delta t/\tau_{(1)})}) \tag{10}$$

where $\tau_{(1)} = R_{p(1)}C_{p(1)}$.

The net v_{DC} variation $\Delta v_{DC(1)}$ at the end of the first time step is derived from Eq. (10), i.e.,

$$\begin{aligned}\Delta v_{DC(1)} &= v_{DC(1)} - v_{DC(0)} = \Delta v^{+}_{DC(1,1)} \\ &= -(R_{S(1)}\bar{I}_{b(1)} + R_{p(1)}\bar{I}_{b(1)}(1 - e^{-(\Delta t/\tau_{(1)})}))\end{aligned} \tag{11}$$

where $\Delta v^{+}_{DC(1,1)}$ denotes the voltage variation caused by the first positive current pulse at the end of the first time interval $t_{(1)}$.

Fig. 5 shows that v_{DC} varies over the first time interval. Since $\bar{P}_{b(1)}$ is assumed constant over the interval Δt, the battery current will in turn vary with v_{DC}. Considering this factor, an inner-loop calculation step is suggested in the numerical solution method step to improve the accuracy of the DC-link voltage calculation. The inner-loop calculation is described as follows. Using $\Delta v_{DC(1)}$ obtained from Eq. (10) as an intermediate variable, one can derive the corresponding battery current as:

$$\bar{I}'_{b(1)} = \frac{\bar{P}_{b(1)}}{v_{DC(1)}} \tag{12}$$

Then update $\bar{I}_b$ by taking the average value of $\bar{I}_b$ from (9) and $\bar{I}'_{b(1)}$ from Eq. (12). One then recalculates $\Delta v_{DC(1)}$ using Eq. (11) and $v_{DC(1)}$ through Eq. (10) with the new $\bar{I}_b$. The above improved battery current and terminal voltage calculation procedure is repeated until $v_{DC(1)}$ convergences. Since it has been known that the battery time-constant τ is much larger than the step-size Δt, it is envisaged that this inner-loop calculation will only result in relatively minor corrections in $\bar{I}_b$ during the iterative process. Hence, convergence can be attained rather quickly.

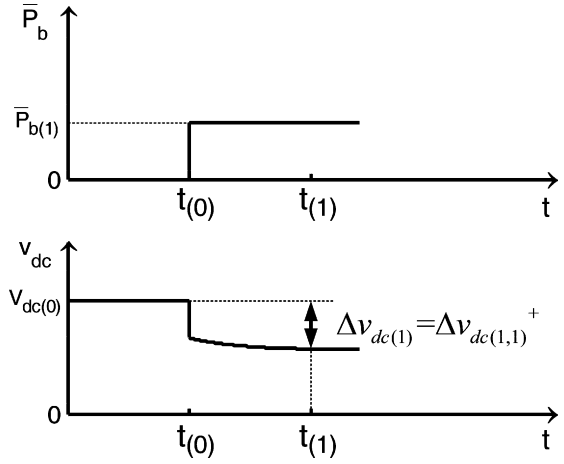

Fig. 5. Estimation of DC-link voltage at end of first time interval.

From the start of the second time interval, i.e., $t > t_{(1)}$, $\bar{P}_{b(2)}$ is introduced as shown in Fig. 6(b). A new battery current step change $\bar{I}_{b(2)}$ is introduced where

$$\bar{I}_{b(2)} = \frac{\bar{P}_{b(2)}}{v_{DC(1)}}$$

$v_{DC(1)}$ is obtained from Eq. (10). To simulate completely the net effect of the first pulse, however, it is necessary to combine the effects shown in Fig. 6(a) with those of Fig. 6(c), i.e., to introduce a negative current step of magnitude $\bar{I}_b$ at the start of the second time interval, as shown in Fig. 6(c). This negative step current produces a voltage response at the end of the second time interval thus

$$\Delta v^{-}_{DC(1,2)} = R_{S(1)}\bar{I}_{b(1)} + R_{p(1)}\bar{I}_{b(1)}(1 - e^{-(\Delta t/\tau_{(1)})}) \tag{13}$$

where $\Delta v^{-}_{DC(1,2)}$ denotes the voltage variation caused by the negative step current at the end of the second time interval $t_{(2)}$. In Eq. (13), it is assumed the negative step current has the same BESS parametric values as that of a positive step current of the same magnitude.

Hence, at the end of the second time step, the BESS voltage variations caused by the positive step currents $\bar{I}_b$ and $\bar{I}_b$ are:

$$\Delta v^{+}_{DC(1,2)} = -(R_{S(1)}\bar{I}_{b(1)} + R_{p(1)}\bar{I}_{b(1)}(1 - e^{-(2\Delta t/\tau_{(1)})}))$$

$$\Delta v^{+}_{DC(2,2)} = -(R_{S(2)}\bar{I}_{b(2)} + R_{p(2)}\bar{I}_{b(2)}(1 - e^{-(\Delta t/\tau_{(2)})}))$$

where $R_{S(2)}$, $R_{p(2)}$ and $C_{p(2)}$ are the BESS parameters corresponding to a current step change of magnitude $\bar{I}_b$ and $\tau_{(2)} = R_{p(2)}C_{p(2)}$. At the same time, the negative step current produces the voltage change $\Delta v^{-}_{DC(1,2)}$ as shown in Eq. (13). Hence, the battery terminal voltage variation at the end of the second time step is:

$$\Delta v_{DC(2)} = \Delta v^{+}_{DC(1,2)} + \Delta v^{+}_{DC(2,2)} + \Delta v^{-}_{DC(1,2)}$$

and v_{DC} at $t_{(2)}$ is

$$v_{DC(2)} = v_{DC(0)} + \Delta v_{DC(2)} \tag{14}$$

Having obtained $v_{DC(2)}$ from Eq. (14), the same inner-loop updating procedure described earlier for $\bar{I}_b$ to calculate Δv_{DC} over the first time interval can also be applied until $v_{DC(2)}$ convergences.

The above v_{DC} calculation procedure is repeated over the interval T. In general, at the kth interval, $v_{DC(k)}$ is determined by the following equations:

$$v_{DC(k)} = v_{DC(0)} + \sum_{M=1}^{k} \Delta v^{+}_{DC(M,k)} + \sum_{M=1}^{k-1} \Delta v^{-}_{DC(M,k)} \tag{15}$$

where

$$\begin{aligned}\Delta v^{+}_{DC(M,k)} = &-(R_{S(M)}\bar{I}_{b(M)} + R_{p(M)}\bar{I}_{b(M)} \\ &\times (1 - e^{-((k-M+1)\Delta t/\tau_{(M)})}))\end{aligned} \tag{16}$$

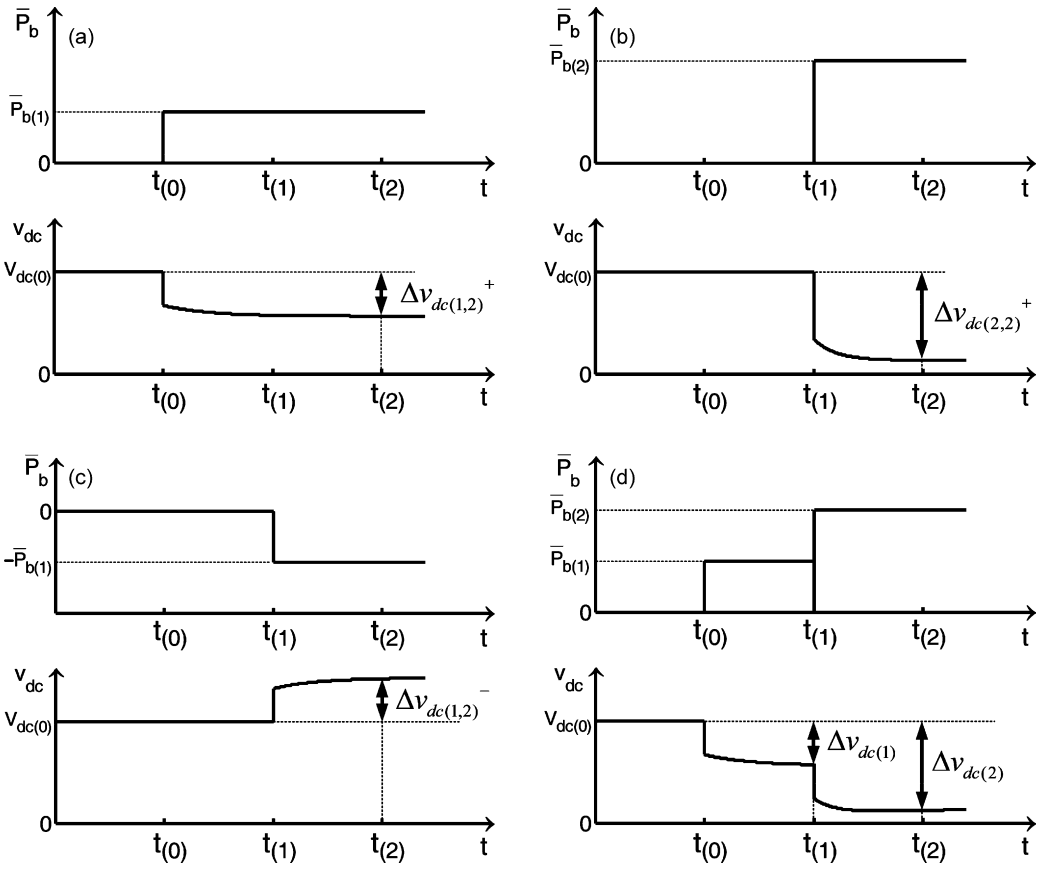

Fig. 6. Estimation of DC-link voltage at end of second time interval.

$$\Delta v^{-}_{\mathrm{DC}(M,k)} = R_{S(M)}\bar{I}_{b(M)} + R_{p(M)}\bar{I}_{b(M)}(1 - \mathrm{e}^{-((k-M)\Delta t/\tau_{(M)})}) \tag{17}$$

$R_{S(M)}$, $R_{p(M)}$ and $C_{p(M)}$ are the BESS parameters corresponding to a current step $\bar{I}_{b(M)}$ and $\tau_{(M)} = R_{p(M)}C_{p(M)}$, $k = 2, 3, \ldots, N$.

Combining Eqs. (10) and (15), one can obtain general expressions for determining v_{DC} at the end of the kth time step as:

$$v_{\mathrm{DC}(k)} = \begin{cases} v_{\mathrm{DC}(0)} + \Delta v_{\mathrm{DC}(1)} & k = 1 \\ v_{\mathrm{DC}(0)} + \displaystyle\sum_{M=1}^{k} \Delta v^{+}_{\mathrm{DC}(M,k)} + \sum_{M=1}^{k-1} \Delta v^{-}_{\mathrm{DC}(M,k)} & k = 2, 3 \ldots N \end{cases} \tag{18}$$

where $\Delta v_{\mathrm{DC}(1)}$, $\Delta v^{+}_{\mathrm{DC}(M,k)}$ and $\Delta v^{-}_{\mathrm{DC}(M,k)}$ are calculated using Eqs. (11), (16) and (17), respectively.

2.6. BESS capacity determination

It is now clear that the BESS not only compensates for the balance of the power between the constant-power load demand and that supplied by the upstream utility system, but also ensures that supply quality to the load does not deteriorate.

Also, as explained in Section 2.2, when a fault occurs and the buffer is switched to the constant-impedance control mode, power has to be extracted from the buffer BESS to meet the balance of the power demanded by the downstream constant-power load. Discharging power from the BESS will consequently depress the BESS terminal voltage v_{DC}. If the BESS capacity is insufficient, v_{DC} may be forced to drop below its set lower limit $v_{\mathrm{DC,lower}}$. As described in Section 2.3, this is not acceptable. One could increase the BESS capacity to prevent v_{DC} from falling below $v_{\mathrm{DC,lower}}$. This can be achieved by adding additional strings of battery cells. From Section 2.4, increasing the number of strings n will correspondingly reduce the internal resistances R_S and R_p, whereas the capacitance C_p will increase. For a given P_b, the discharge current will be reduced, and hence, the terminal voltage deviations will be less.

Over the transient interval when the power system readjusts the power flows and network voltages, it is also likely that the amount of power supplied by the upstream source can be greater than that demanded by the downstream constant-power load. Under such circumstances, the surplus power will be absorbed by the BESS and v_{DC} increases. Hence, the capacity of BESS should also be sufficiently large to guarantee v_{DC} does not exceed the pre-set upper limit $v_{\mathrm{DC,upper}}$. Again, this can be achieved by increasing the number of parallel branches of the cells. The capacity of the BESS may therefore be determined based on the worst fault disturbance condition for which the buffer scheme is designed.

3. Simulation results

To illustrate the design procedure of the previous section, the simple power system depicted in Fig. 1 was simulated using the well-known package PSCAD. In this example, a single-circuit radial link between Buses 1 and 2 is assumed. The line and generator parameters used for the simulations are listed in Appendix (A). Data is taken from references [13,14]. The AC1A type excitation and mechanical–hydraulic controlled (MHC) governor systems [14] are also included in the generator systems. The power flow pattern at a nominal condition is such that G_1 has a generation of 1575 MW and G_2 is of 75 MW. The load levels at Buses 1 and 2 are 1500 and 150 MW, respectively. Hence, 75 MW is imported from Bus 1 into Bus 2 through the transmission link.

Assume half of the loads at Buses 1 and 2 are essential (super-premium) and are to be protected by the power buffers. By assuming a line fault condition, the response of the power system was studied and from the power flows and Eq. (6), P_b on the BESS can be obtained for both the buffers. v_{DC} of the respective buffer is calculated using the computational method described in Section 2.

3.1. A temporary mid-line three-phase fault

A temporary 10-cycle three-phase-to-ground fault event at the midpoint of the transmission line is examined first. By varying the buffer switching pattern to realize either constant-impedance or constant-power modes on the basis of the variations of P_{12} about the pre-fault transfer level of 75 MW, it is intended to demonstrate that the stability of the power system is improved. As stated earlier, Power Buffer 2 is switched into a constant-impedance mode during the fault occurrence. $BESS_2$ discharges to compensate for the mismatched power between the constant power S_2 demanded and that supplied by the upstream sources. The power profile of $BESS_2$ is calculated using Eq. (6) and is given in Fig. 7(a), in which positive values denote power discharging from $BESS_2$ while negative ones indicate $BESS_2$ is being charged. At Buffer 1, there is a negligible amount of power exchange between $BESS_1$ and the external system. This is because the constant mechanical power generated by G_1 is greater than that demanded by the load connected to Bus 1. Hence, Buffer 1 operates under a constant-power mode during the fault to reduce acceleration of the G_1 rotor. Therefore, only the performance and simulation results of Buffer 2 are described as follows.

The BESS cells have the parametric values given in Table 1. Assume the modulation indices of the power buffers are at the typical value of 0.8 and the initial DC-link voltage of Power Buffer 2 is 269.44 kV. Therefore, each BESS branch will be composed of 40,825 cells since each cell is rated at 6.6 V. Using the computational procedure described in Section 2.5 and based on P_{b_2} shown in Fig. 7(a), v_{DC} is calculated. The time step used is the half-cycle of the power frequency. The v_{DC} so obtained is

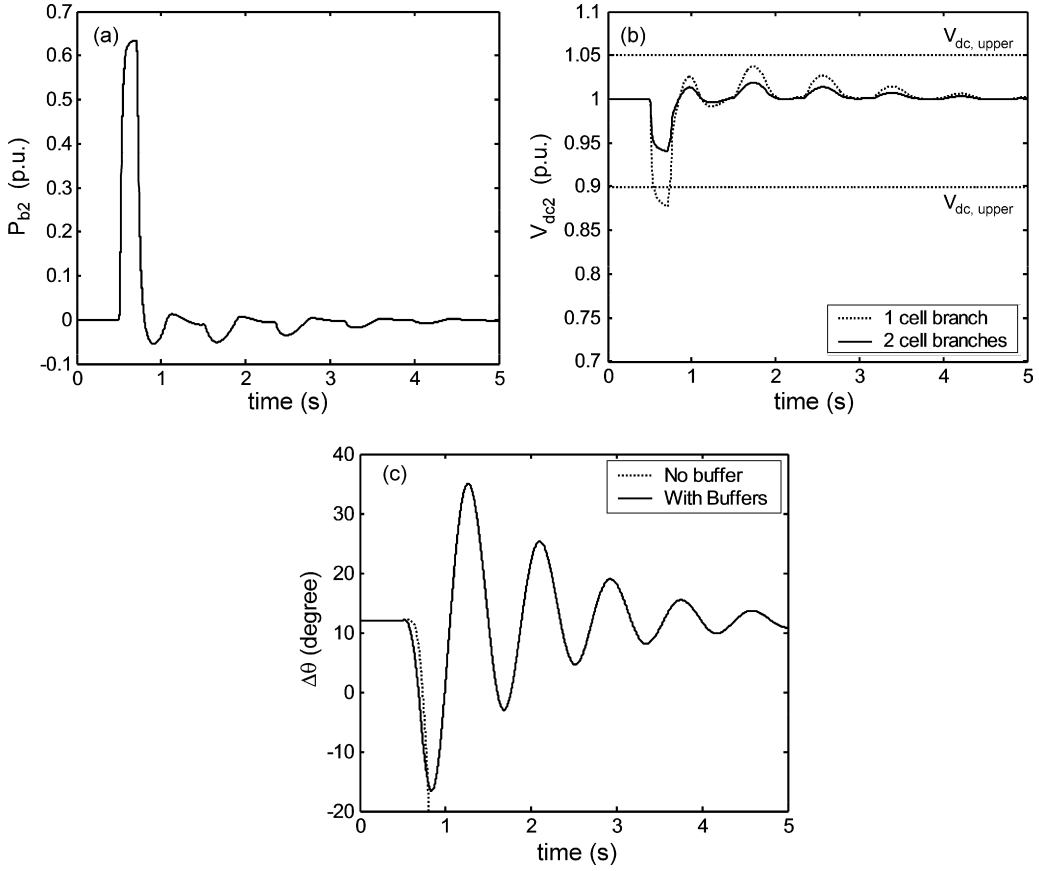

Fig. 7. $BESS_2$ response following temporary 10-cycle three-phase mid-line fault: (a) P_{b_2}, (b) v_{DC_2} and (c) rotor-angle difference $(\theta_1 - \theta_2)$ between G_1 and G_2: with and without power buffers.

shown in Fig. 7(b). In these plots, the base power and DC-link voltage values used are 100 MW and 269.44 kV, respectively.

For satisfactory operations of the downstream protected loads, assume the DC-link voltage is constrained to operate within the range [0.9, 1.05] p.u. This is a reasonable assumption; for example, adjustable-speed drive systems would only operate satisfactorily within this range [15]. Assume $BESS_2$ has only one string of the cells. From Fig. 7(b), it is seen that in supporting the load demand S_2, v_{DC_2} is depressed below the set lower limit over the initial stage of the fault disturbance. In this case, S_2 will not be supplied at a voltage level that is acceptable for satisfactory continuous operation.

One can attempt to increase $BESS_2$ capacity by adding one more string of the cells. The corresponding v_{DC_2} profile for the two-string $BESS_2$ is also shown in Fig. 7(b). The two-branch $BESS_2$ is observed to be capable of maintaining v_{DC_2} well within the limits. Therefore, the capacity of $BESS_2$ is determined to consist of two strings because in this instance the DC-link voltage is improved and the voltage quality of S_2 is of an acceptable level.

The effect of the power buffers in enhancement of the transient stability can be seen from Fig. 7(c). As shown by the dotted line that corresponds to the case without buffers incorporated, the rotor-angle difference continues to increase monotonically and the system loses synchronism consequently. When the proposed buffer operation is utilized, however, instability is avoided as can be seen from the solid line in Fig. 7(c). It clearly demonstrates that the buffer systems do function as effective network system dampers or stabilizers.

An interesting observation can be made from Fig. 7(b). It is seen that the v_{DC} post-fault steady-state level remains the same as that of the pre-fault level, although it is clear from Fig. 7(a) that there is a net export of energy from $BESS_2$ to the load over the period of study. With the net discharge of energy from the BESS, the battery terminal voltage is expected to decrease in the longer term because its internal emf (E_b) decreases as the BESS state-of-discharge (SoD) increases [10]. In the present work, it has been assumed that E_b remains constant over the fault incident. For longer term study of (say) several tens of seconds, it is necessary to include the SoD effect into the analysis.

3.2. A temporary three-phase fault close to Bus 2

The capacity of the $BESS_2$ determined for the midpoint fault condition is evaluated for its suitability for the same temporary three-phase 10-cycle fault event, but is now located at a distance corresponding to 1 km from Bus 2. P_{b_2} for this case is given in Fig. 8(a), while the v_{DC} computed is shown in Fig. 8(b).

Comparing P_{b_2} shown in Fig. 8(a) with that in Fig. 7(a), it is observed that with the fault occurring closer to Bus 2, $BESS_2$ has to increase its discharged power. Indeed, as shown in Fig. 8(b) and under such a fault condition, $BESS_2$ with one cell string would result in v_{DC_2} not only falling below the lower limit over the fault interval but also subsequently rising momentarily above

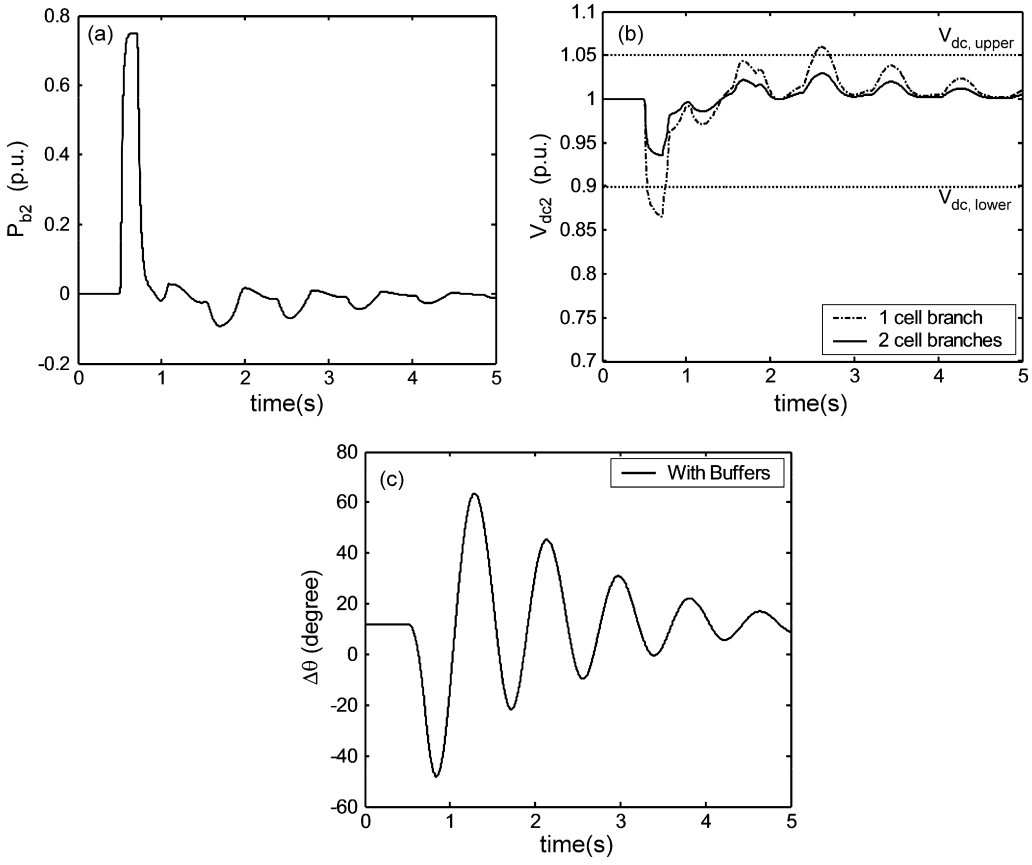

Fig. 8. $BESS_2$ response following temporary 10-cycle fault 1 km from Bus 2: (a) P_{b_2}, (b) v_{DC_2} and (c) rotor-angle difference.

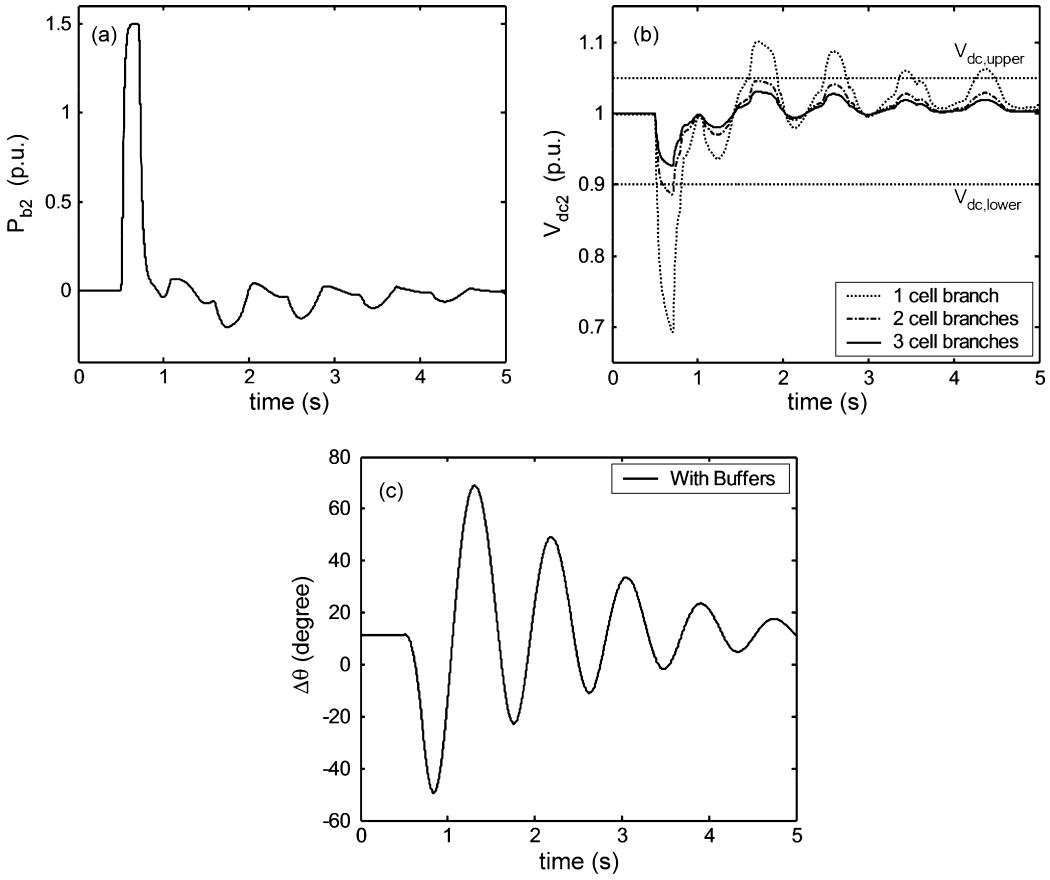

Fig. 9. $BESS_2$ response of 100% of constant power loads connected at both ends under temporary three-phase fault 1 km from Bus 2: (a) P_{b_2}, (b) v_{DC_2} and (c) rotor-angle difference.

its upper limit during the system recovery period. The estimated v_{DC_2} when the $BESS_2$ consists of two cell strings is also given in Fig. 8(b) and is seen to produce satisfactory performance. Again, as shown in Fig. 8(c), the power system is transiently stable with such a load buffer scheme.

3.3. Further discussion of results

One more interesting issue pertains to the proportion of the super-premium loads. Instead of assuming the load connected to each bus should consist of equal amounts of constant-power super-premium load and constant-impedance load, additional studies have been carried out when 100% of the loads are taken to be super-premium and are to be protected by the buffers. Hence, the pre-fault load capacity of S_1 is 1500 MW and that of S_2 is 150 MW.

For the purpose of comparison, the simulation studies corresponding to the above-described load pattern under temporary 10-cycle three-phase fault cases at mid-line and 1 km from Bus 2, respectively, are repeated. Due to the limitation of space, only the results for a fault that is 1 km from Bus 2 are given in Fig. 9. For this fault case, the power profile of $BESS_2$ is shown in Fig. 9(a), from which it is found that the output power of $BESS_2$ has to be increased due to the increase in the proportion of the constant-power load at Bus 2. Therefore, the capacity of $BESS_2$ has to be enlarged. This point can be seen from the DC-link profile given in Fig. 9(b), where even for the two-string BESS, v_{DC} still violates the lower and upper v_{DC} limits during both fault and post fault. One additional string is added to $BESS_2$ and the resulting v_{DC} profile is shown as the solid line in Fig. 9(b). The improved transient stability with the help of the power buffer can be seen from the rotor-angle difference profile in Fig. 9(c).

From the results of the numerical examples, it is not surprising to note that as the fault event is moved electrically closer to the load-buffer or when the proportion of the super-premium loads is increased, it is necessary to increase the BESS capacity to cater for the constant-power demand of the loads. Therefore, the capacities of the BESSs within the power buffers have to increase with increasing penetration of the super-premium constant-power loads in the network.

4. Conclusions

From the basic function of power buffers for voltage quality improvement, an extension of the buffer application to enhance power system stability has been explored. The focus of the investigation is on the design of the BESS of the buffers. When a buffer operates under a constant-impedance mode, the BESS discharges or absorbs power. This will cause its terminal voltage to deviate. A computational technique to determine the terminal voltage has been developed based on the battery power discharged or absorbed. As the BESS is connected across the buffer

DC-link, the voltage deviations will have an impact on the voltage quality of the downstream protected load. The proposed method allows a suitable capacity of the BESS to be determined so that acceptable voltage quality for the protected load will be obtained. Numerical results show that the capacity of the BESS increases with the amount of the protected load and the severity of the fault. Through the implementation of the proposed power buffer scheme, the stability of the network will also be enhanced under system disturbance conditions.

Appendix A

A.1. (A) Line parameters used in simulations [13]

System voltage = 132 kV, nominal frequency = 50 Hz, line length = 200 km, $r = 0.068\ \Omega\ \mathrm{km}^{-1}$, $x = 0.404\ \Omega\ \mathrm{km}^{-1}$, $b = 7.59\mathrm{E}{-6}\ \mathrm{S\ km}^{-1}$.

A.2. (B) Equivalent machine parameters used in simulations [14]

G_1: $S_N = 2000$ MVA, $H = 4.0$ s, $X_d = 1.00$ p.u., $X'_d = 0.30$ p.u., $X''_d = 0.20$ p.u., $X_q = 0.60$ p.u., $X''_q = 0.20$ p.u., $X_a = 0.12$ p.u., $T'_{d0} = 5.00$ s, $T''_{d0} = 0.08$ s, $T'_{q0} = -$, $T''_{q0} = 0.12$ s.

G_2: $S_N = 100$ MVA, $H = 4.0$ s, $X_d = 2.00$ p.u., $X'_d = 0.25$ p.u., $X''_d = 0.20$ p.u., $X_q = 0.50$ p.u., $X''_q = 0.20$ p.u., $X_a = 0.15$ p.u., $T'_{d0} = 6.00$ s, $T''_{d0} = 0.03$ s, $T'_{q0} = 0.60$ s, $T''_{q0} = 0.06$ s.

A.3. (C) AC1A type exciter and regulator parameters used in simulations (p.u.) [14]

$T_R = 0.0$, $K_A = 400.0$, $T_A = 0.02$, $T_B = 0.0$, $T_C = 0.0$, $K_F = 0.03$, $T_F = 1.0$, $K_E = 1.0$, $T_E = 0.8$, $K_D = 0.38$, $K_C = 0.2$, $V_{R_{\mathrm{MAX}}} = -6.03$, $V_{R_{\mathrm{MIN}}} = -5.43$, $V_{A_{\mathrm{MAX}}} = 14.5$, $V_{A_{\mathrm{MIN}}} = -14.5$.

A.4. (D) MHC governor parameters used in simulations [14]

G_1: $T_P = 0.05$ s, $K_S = 5.0$, $T_G = 0.2$ s, $R_P = 0.04$, $R_T = 0.4$, $T_R = 5.0$, $G_{\mathrm{MAX}} = 1.0$ p.u., $G_{\mathrm{MIN}} = 0.0$ p.u., $R_{\mathrm{max,open}} = 0.16$ p.u. s^{-1}, $R_{\mathrm{max,close}} = 0.16$ p.u. s^{-1}.

G_2: $K_G = 20$, $T_{SR} = 0.1$ s, $T_{SM} = 0.2$ s, $T_{SI} = 0.2$ s, $L_{C1} = 0.2$, $L_{C2} = -0.5$, $L_{I1} = 0.2$, $L_{I2} = -0.5$.

References

[1] V. Knyazkin, C.A. Canizares, L.H. Soder, IEEE Trans. Power Syst. 19 (2004) 1023–1031.
[2] L.M. Hajagos, B. Danai, IEEE Trans. Power Syst. 13 (1998) 584–592.
[3] IEEE Task Force Report, IEEE Trans. Power Syst. 8 (2) (1993) 472–482.
[4] D.L. Logue, P.T. Krein, Proc. IEEE PESC (2000) 973–978.
[5] X.Y. Wang, D.M. Vilathgamuwa, S.S. Choi, Proc. IEEE PES General Meeting (2006) 1–8.
[6] S.S. Choi, X.M. Jia, IEEE Trans. Power Syst. 14 (1999) 1279–1284.
[7] N.G. Hingorani, IEEE Spectr. 32 (1995) 41–48.
[8] Y.Q. Zhan, S.S. Choi, D.M. Vilathgamuwa, IEEE Trans. Power Del. 21 (2006) 296–304.
[9] P.F. Ribeiro, B.K. Johnson, M.L. Crow, A. Arsoy, Y.L. Liu, Proc. IEEE 89 (2001) 1744–1756.
[10] C.J. Zhan, X.G. Wu, S. Kromlidis, V.K. Ramachandaramurthy, M. Barnes, N. Jenkins, A.J. Ruddell, IEE Proc. Gener. Transm. Distribut. 150 (2003) 175–182.
[11] Y.H. Kim, H.D. Ha, IEEE Trans. Ind. Electron. 44 (1997) 81–86.
[12] A.J. Salkind, P. Singh, A. Cannone, T. Atwater, X. Wang, D. Reisner, J. Power Sources 116 (2003) 174–184.
[13] B.M. Weedy, Electric Power Systems, fourth ed., John Wiley & Sons, New York, 1998, pp. 114–115.
[14] P. Kundur, Power System Stability and Control, vol. 153, McGraw Hill, New York, 1994, pp. 364–399.
[15] J.L. Duran-Gomez, P.N. Enjeti, B.O. Woo, IEEE Trans. Ind. Appl. 35 (1999) 1440–1449.